A HYBRID APPROACH FOR MITIGATING TRANSIENT AND PERMANENT FAULTS IN MEMORY SUBSYSTEMS USING EDC, ECC, AND BIST

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ABSTRACT

This paper presents a hybrid fault-tolerant 64×16 Random Access Memory (RAM) subsystem designed to mitigate both transient and permanent faults using a combination of Error Detection Code (EDC), Error Correction Code (ECC), and Built-In Self-Test (BIST) techniques. Developed in Verilog HDL and verified with a System Verilog-based environment, the architecture integrates multiple resilience strategies to enhance memory reliability in safety-critical and high-dependability applications. The ECC module implements a Hamming-based SEC-DED (Single Error Correction – Double Error Detection) scheme, encoding 16-bit input data with five parity bits to generate a 21-bit output, enabling real-time correction of single-bit errors and detection of double-bit faults. The EDC mechanisms provide additional lightweight detection during normal operation, offering fast identification of error patterns before correction or isolation. The BIST controller autonomously initiates test routines by writing known patterns to memory, reading them back, and comparing the results to identify permanent faults without requiring external testing hardware. The top-level architecture seamlessly switches between normal operation and self-test modes, ensuring uninterrupted functionality. Extensive simulation using randomized and fault-injection scenarios confirms the design's robustness, demonstrating reliable error detection and correction across varying fault conditions. This hybrid solution provides an efficient and scalable framework for fault mitigation in modern memory subsystems.

II.INTRODUCTION

Memory plays a critical role in System-on-Chip (SoC) architectures, serving as the backbone for data storage, retrieval, and processing in digital systems. Among various memory types, Static Random Access Memory (SRAM) is widely used due to its high speed and ease of integration with logic components. However, SRAM suffers from high silicon area consumption, which impacts power efficiency and scalability. On the other hand, Dynamic Random Access Memory (DRAM) offers a more compact cell structure using capacitors but demands

periodic refreshing, increasing design complexity and power overhead. As digital systems become more compact and operate in increasingly harsh environments—such as automotive, aerospace, and medical electronics—ensuring memory reliability becomes a major concern. Memory subsystems are particularly vulnerable to both transient faults, caused by radiation or voltage fluctuations, and permanent faults, due to aging, wear-out, or manufacturing defects. These faults can compromise system performance and data integrity, posing serious risks in safety-critical applications. To address these reliability challenges, hybrid fault mitigation techniques have emerged as a promising solution. Error Detection Code (EDC) offers lightweight mechanisms to identify data corruption, while Error Correction Code (ECC), such as Hamming SEC-DED schemes, enables automatic correction of single-bit errors and detection of multi-bit faults. Built-In Self-Test (BIST) further enhances system robustness by enabling autonomous detection of permanent faults through predefined test patterns, eliminating the need for external testing equipment. This paper explores a hybrid approach that integrates EDC, ECC, and BIST into a fault-tolerant memory subsystem. The goal is to strike a balance between performance, area, and power efficiency while ensuring high reliability in environments prone to both transient and permanent faults.

III.LITERATURE SURVEY

Transparent BIST for ECC-Based Memory Repair – Michael Nicolaidis, Panagiota Papavramidou (2013) This work introduces a novel BIST architecture that operates transparently alongside ECC-enabled memory systems. The approach allows in-field memory testing without disrupting ECC functionality, ensuring continuous system operation. The BIST framework integrates a smart repair algorithm that works in synergy with ECC to handle both permanent and transient faults effectively. Particularly suited for embedded and safety-critical systems, this method enhances memory reliability and reduces downtime, making it a practical solution for real-time environments where memory faults must be addressed without halting system operations.

A Memory Yield Improvement Scheme Combining BIST and ECC – Tze-Hsin Wu et al. (2012) This study proposes the ECC-Enhanced Memory Repair (EEMR) scheme to boost memory manufacturing yield by integrating ECC with Built-In Redundancy Analysis (BIRA). The method involves a sequential repair strategy where ECC and BIRA cooperate to detect and correct faults. The scheme adapts to various ECC configurations and fault distributions, demonstrating flexibility and scalability. With over 2% yield improvement observed across 100,000 memory instances, this hybrid technique proves efficient for commercial

memory arrays where both yield and post-deployment reliability are crucial.

Evaluating Built-in ECC of FPGA On-Chip Memories for Fault Mitigation – Behzad Salami et al. (2019) This paper evaluates the fault-tolerant capabilities of built-in SEC-DED ECC in FPGA Block RAMs (BRAMs), particularly under voltage underscaling conditions. The results show that ECC successfully corrects over 90% of errors and detects an additional 7%, thereby significantly improving memory robustness in low-power environments. This is especially important in AI accelerators and edge computing devices where energy efficiency is critical. The study confirms ECC's effectiveness as a lightweight and power-efficient solution for mitigating transient faults in reconfigurable hardware platforms.

IV.PROPOSED IMPLEMENTATION

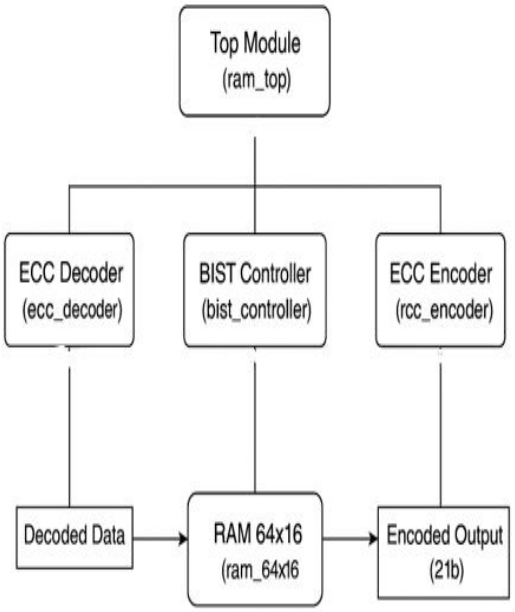

Fig:1 BLOCK DIAGRAM

The proposed system presents a hybrid fault-tolerant memory architecture designed to enhance the reliability and testability of a 64×16 Random Access Memory (RAM) subsystem. This architecture integrates three core components—Error Detection and Correction (EDC/ECC) modules and a Built-In Self-Test (BIST) controller.

At the heart of the system is the ram_top module, which acts as the primary control unit coordinating data flow and operational modes among the integrated submodules. The architecture is composed of the following key components:

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Hamming-based SEC-DED (Single Error Correction – Double Error Detection) scheme. It processes incoming 16-bit data and appends five parity bits, generating a 21-bit encoded word. This encoded data is written to memory, providing the first line of defense against data corruption. ECC Decoder: Connected to the output path of the RAM, the ECC Decoder retrieves the 21-bit encoded data, recalculates the syndrome, and performs correction for single-bit errors or flags double-bit errors. It outputs clean, corrected 16-bit data to the user, ensuring data integrity during read operations. BIST Controller: The Built-In Self-Test (BIST) Controller is responsible for performing autonomous memory testing. It injects known test patterns into the memory, reads the stored values, and compares them with expected results.

RESULTS

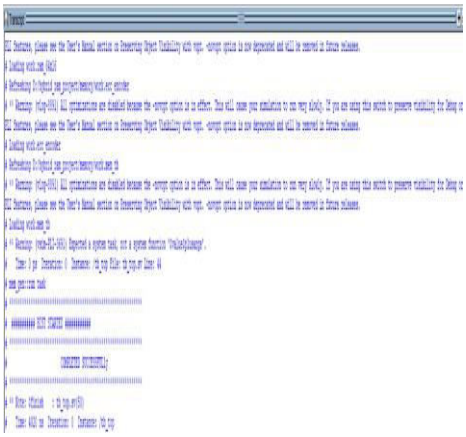

Fig: 2(a) write and read operations

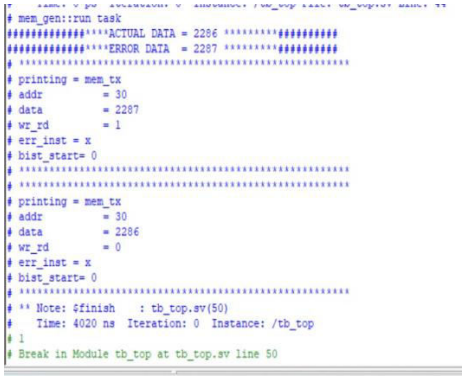

Fig: 2 (b)write and read operations

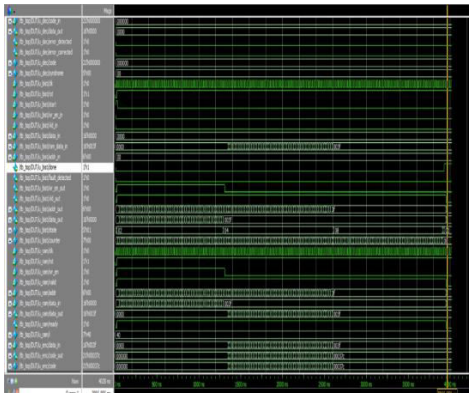

Fig: 3(a) wave form simulation

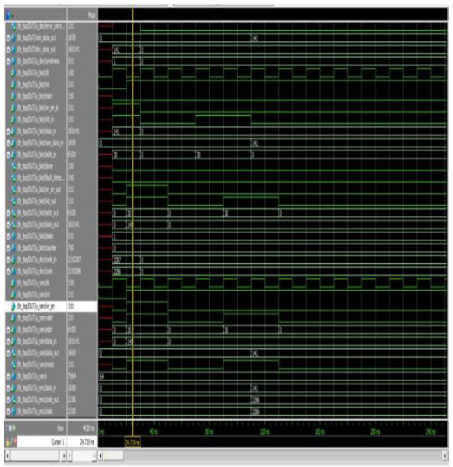

Fig: 3(b) wave form simulation

CONCLUSION

The proposed hybrid memory subsystem demonstrates a robust and efficient solution for mitigating both transient and permanent faults through the integration of Error Detection and

Correction (EDC/ECC) mechanisms and Built-In Self-Test (BIST) capabilities. The implementation of a 64×16 fault-tolerant RAM using the Hamming SEC-DED ECC scheme enables reliable correction of single-bit errors and detection of double-bit faults during runtime. Complementing this, the BIST controller provides autonomous and periodic testing to identify permanent hardware faults without the need for external test equipment. The architecture's dual-mode functionality—supporting both normal operation and self-test—enhances flexibility and fault coverage. Extensive validation through SystemVerilog-based simulation, including fault injection and random testing scenarios, confirmed the system's reliability and correctness under fault conditions. This hybrid approach not only ensures high data integrity but also reduces system downtime and maintenance overhead

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